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JAN 77 G L VARNELL, R A WILLIAMSON DAAB07-76-C-8105
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First Quarterly Report

IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY

Period Covered
1 July 1976 – 1 October 1976

Contract No. DAAB07-76-C-8105

Procurement and Production Directorate
U.S. Army Electronics Command
Fort Monmouth, New Jersey 07703

Texas Instruments Incorporated
P.O. Box 5012
Dallas, Texas 75222

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(10) Gilbert L. Varnell, John L. Bartelt, Claude D. Winborn
Ronald A. Williamson, Richard J. Dexter
Terry L. Brewer, Roger A. Robbins

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A program to implement e-beam writing technology for fabrication of microcircuits has been initiated this quarter. The technical and economic impact of electron-beam direct slice printing will be demonstrated on 256-bit bipolar RAMs utilizing ~~Texas Instruments~~ an electron-beam machine (EBMIIIA). Earlier this year a new high-speed interface was installed on EBMIII to allow up to 5 μm/μs scan rates and 0.5 μm line spacings. This corresponds to a data rate of 10 MHz at 0.5 μm spacings and 20 MHz at 0.25 μm spacings. The conceptual design of an automatic slice loading system has been completed. This would allow slice loading from standard boats under computer control with no operator intervention. This will reduce total cycle time and reduce system downtime since at present the entire chamber is exposed to the atmosphere during slice loading.

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The proposed IC for this contract is a single monolithic integrated circuit containing a 256-word by 1-bit fully static random access nondestructive readout memory. The memory if fully decoded requires only 8 address lines to select one of 256 storage locations. An additional line, write enable, is provided to enable the memory to modify the stored data. Separate Data Input and Data Output lines are provided for minimum interaction between input and output functions. Three chip enable lines are provided to simplify the decoding required to achieve the desired system.

IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY

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Dr. G. L. Varnell
Mr. R. A. Williamson
Dr. T. L. Brewer
Dr. J. L. Bartelt
Dr. R. J. Dexter
Dr. R. A. Robbins
Mr. C. D. Winborn

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I
PURPOSE

The overall objective of the program is to implement e-beam writing technology for the fabrication of microcircuits. The technical and economic impact of electron beam direct slice printing will be demonstrated on 256-bit bipolar RAMs. The elimination of mask masters, masks and the masking process will eliminate the most significant source of yield loss. This will permit greater circuit design complexity and flexibility which will lead to lower device costs with increased reliability. The complete implementation program is divided into three tasks. Task A, Yield Improvement Through Direct E-Beam Writing, is directed toward developing the manufacturing technology required for e-beam writing with existing equipment and existing resist processes and demonstrating the yield benefits of this technique. Task B, Cost Reduction for E-Beam Writing Through High Speed Resist Implementation, is directed toward implementing identified high speed e-beam resists in order to significantly decrease cycle time and thus reduce the IC bar cost. Task C, Cost Reduction for E-Beam Writing Through Automatic Beam Diameter Control and Automatic Handling, is directed toward utilizing EBMIII's capability of computer-controlled beam size (large and small) on high density circuit ($\leqslant$0.1 mil) geometries. This program also includes implementation of an automated handling system for slices to reduce cycle time and thus further reduce bar cost.

SECTION II
NARRATIVE AND DATA

A. ELECTRON BEAM WRITING SYSTEMS

1. Introduction

Electron-beam writing systems using a computer to generate the pattern by controlling the deflection of the electron beam are attractive for rapid device design, mask fabrication, and high yield device processing because they permit delineation of microcircuit patterns from computer data. These e-beam systems are also advantageous for high frequency and high packing density microcircuit fabrication because they permit higher resolution and better alignment accuracy than achievable with conventional photolithographic techniques.

Texas Instruments has been engaged in a research and development program since 1966 to utilize electron beams as a method of delineating microcircuit patterns. On this program, fully computer-controlled electron-beam pattern generators have been developed to advance the economic feasibility of electron-beam writing. Table I lists the completion dates, usage, and advantages of these instruments.

Discrete device fabrication by electron-beam writing (EBMI) has been demonstrated by Texas Instruments on a previous contract.[1] C-band transistors were fabricated using fully computer-controlled electron-beam pattern generation and registration. The transistors delivered actually exceeded the contract specifications of 8-dB gain and 5.5-dB noise figure at 6 GHz. Tests on EBMI showed level-to-level registration within ±0.2 μm on 98% of the field. Resolution was 0.5 μm over the entire field. Processes were developed for oxide and Mo-Au definition utilizing polymethylmethacrylate and polystyrene electron resists. This e-beam writing system (EBMI) was severely limited in cost effectiveness by the restricted throughput of this serial exposure technique. For this reason, electron-beam writing instruments have been developed that allow accurate, high speed, large area microcircuit pattern delineation of photomasks or wafers.

1. U.S. Army Electronics Command, Contract DAAB05-71-C-3715

Table I. TI Electron-Beam Machine

	Completion	Usage	Advantages
EBMI	1971	Specialty devices	Submicron device geometries and ±0.25 μm reregistration
EBMII	1974	Photomask 10X Reticles	Fast turnaround Higher quality photomask
EBMIIIA	1976	Direct slice printing, VLSI	Resolution Reregistration accuracy Geometry Control Fewer defects

These instruments incorporate most of the principles of the earlier e-beam writing system (EBMI)[2,3] but have several additional features and greatly improved performance. Dynamic focusing and air-core deflection coils designed by computing exact electron trajectories permit delineation of 1.0-μm lines in electron resist over a 6.35 mm X 6.35 mm area. The pattern generating electronics coupled with the electron optical deflection system allows beam writing speeds of up to 5 μm/μs with 0.5 μm beam spacings for geometries ≥2.5 μm (0.1 mil). This writing system combined with a LaB_6 electron gun and a negative or positive electron resist of 2.5 μcoul/cm^2 sensitivity permits pattern writing of standard IC patterns with 20-40% clear or opaque area in 8-16 s/cm^2 plus ≈ 10-20% settling overhead. The overhead in this Vector Write system is due to computer output, beam and DAC settling times. The beam settling times are limited by the eddy currents induced during beam movement. The combination of a commercial laser interferometer, an automatic pattern registration system, stage shift correction circuitry and high speed stepping motors permits master mask overlay accuracy of ±0.5 μm over a 7.5 cm X 7.5 cm array without the use of any fiducial markers on the photomask. For direct slice writing, the automatic pattern registration technique developed on EBMI can be utilized. This will permit ±0.2 μm pattern registration accuracy. A combination of the Automatic Pattern Registration system and laser interferometer control is also available for slice printing to permit only 3-5 sets of fiducial markers per slice.

2. Varnell, G. L., Spicer, D. F. and Rodger, A. C., "E-Beam Writing Techniques for Semiconductor Device Fabrication," 12th Symposium on Electron, Ion, and Laser Beam Technology, Cambridge, Massachusetts, May 1973.

3. Spicer, D. F., Rodger, A. C. and Varnell, G. L., "Computer-Controlled Pattern Generating System for Use with Electron Beam Writing Instruments," 12th Symposium on Electron, Ion, and Laser Beam Technology, Cambridge, Massachusetts, May 1973.

2. Electron-Beam Pattern Generator (EBMIII)

The electron-beam pattern generator developed for microcircuit fabrication is shown in Figures 1, 2, and 3 and a block diagram of the instruments is shown in Figure 4. This instrument (EBMIIIA) incorporates most of the principles of EBMI but has several additional features and greatly improved performance. The electron-beam column has been redesigned and incorporates a new ion-pumped LaB_6 electron gun and a three lens, "shaped beam" electron optics column to provide well-defined beam diameters with approximately uniform current profiles. The mechanical stage is laser interferometer controlled and incorporates semiautomatic material handling. The system computer is a TI980A with 32K of memory and extensive peripherals (magnetic disc, magnetic tape, punched card reader, and TI *Silent 700* data terminal). Improvements have also been made to the electronics and electron optical deflection system for greater reliability and higher speed performance. The major features of EBMIIIA are listed below:

- Scan area (field size) — Up to 6.35 X 6.35 mm
- Line resolution — 6250 Lines at 3 mrads beam semiconvergence angle (1.0 μm over 6.35 mm X 6.35 mm area)

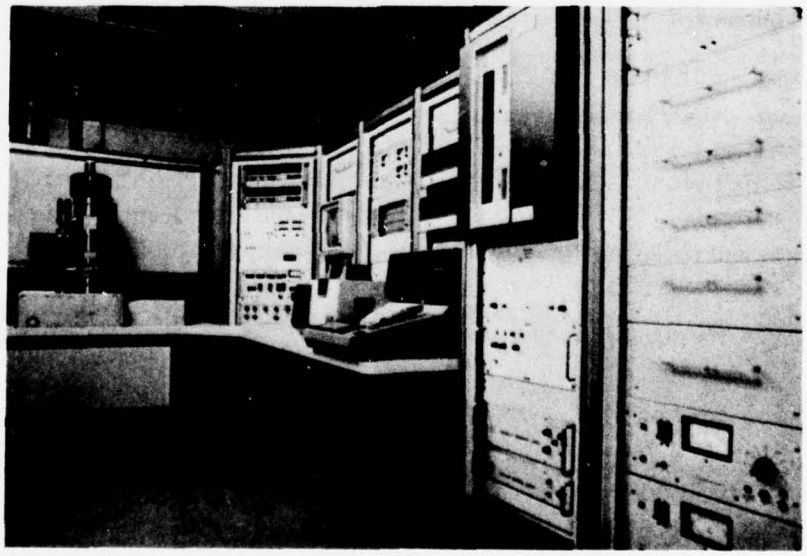


Figure 1. Electron-Beam Slice Printer

• Point resolution (Least significant bit size)	0.125 μm (6.35 X 6.35 mm field)
• Pattern nonlinearity	<0.05% of field size
• Figure drafting	Steered beam
• Beam diameter	Variable from 0.25 μm to 5.2 μm (Computer controlled option of preset "large" or "small" beam)
• Accelerating voltage	15 kV
• Objective lens focal length	7.5 cm
• Scanning speed	Programmable from 40 μm/ms to 5 μm/μs
• Pattern writing time (2.5 μcoul/cm^2 resist) (30% area)	12 s/cm^2 plus 10-20% overhead
• X-Y table stepping speed	1.3 cm/s over 12.5 cm X 12.5 cm
• Direct writing pattern registration accuracy – every bar alignment	±0.25 μm
• Combination laser and fiducial marker alignment – three bar alignment	±0.5 μm
• Data Input	
Complex IC patterns	Magnetic tape after decomposition on IBM 360
Simple devices and test patterns	Card or teletype
• Pattern intermix	Capable of intermix of 50 patterns on a single wafer with equal alignment accuracies
• Pattern generation capability	All normal photomask geometries

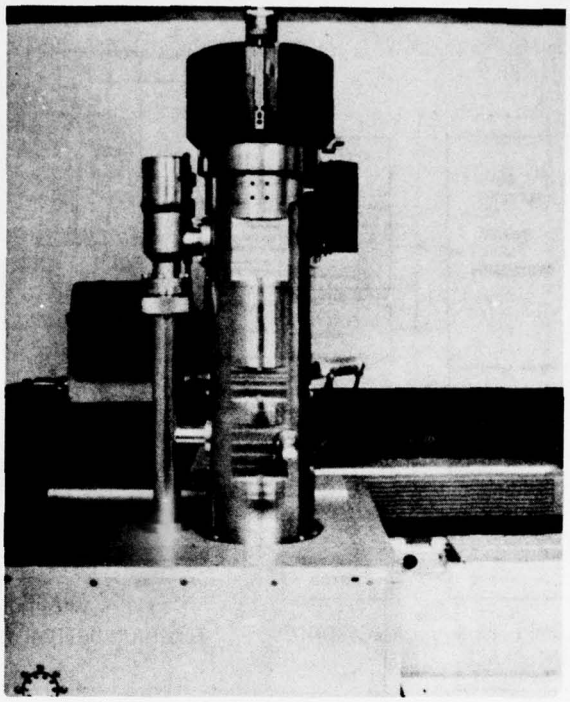


Figure 2. EBMII Electron Optical Column

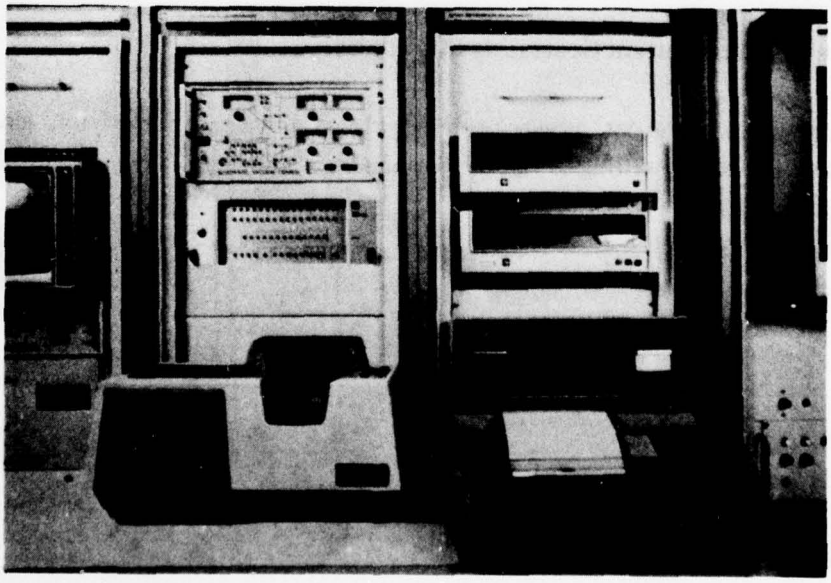


Figure 3. EBMIII Computer and Peripherals

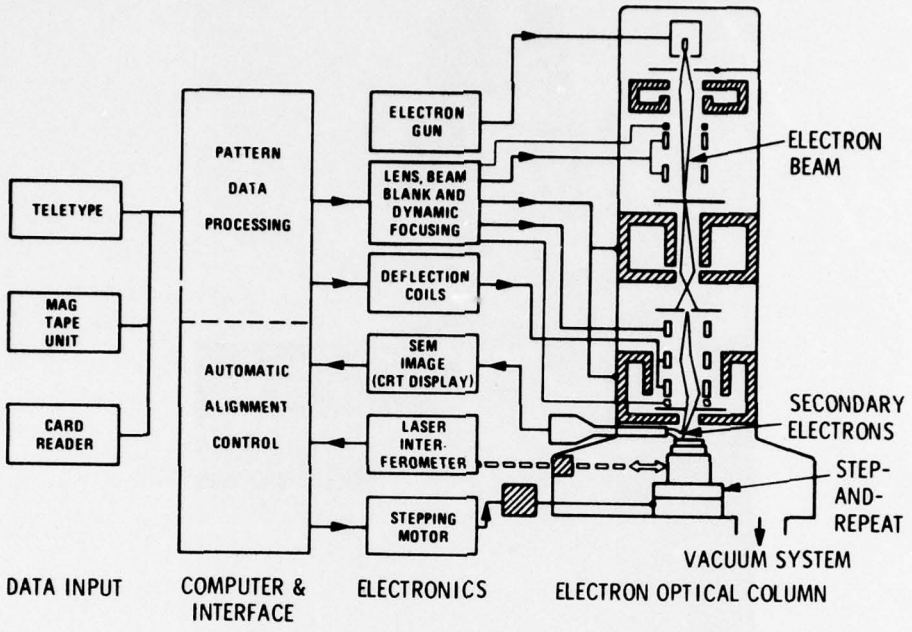


Figure 4. Electron-Beam Pattern Generation Schematic

3. Deflection Coils and Pattern Generating Electronics

The major technical barrier, besides gun brightness and resist sensitivity, which has limited widespread use of e-beam writing is the performance of the deflection system and the pattern generating electronics.

The deflection coils of commercial scanning electron microscopes permit extremely high resolution but at a trade-off of small field coverage. Unacceptable astigmatism, curvature of field, distortion, and nonlinearities occur when the beam is scanned over a large area. A deflection system for microcircuit fabrication should permit 5000 lines resolution (i.e., 1.25 μm over a 6.35 X 6.35 mm field for standard IC devices and 0.5 μm over a 2.5 mm X 2.5 mm field for special devices) and minimal nonlinearity (i.e., <0.1%).

The distortion and nonlinearity requirements of the deflection system for EBMIII were met by writing a computer program to combine the fields from the individual coils, computing the trajectory of the electron beam, and optimizing the coil dimensions by calculating partial-differential coefficients.[2] The resolution requirements over the large field were met by designing a full dynamic focus correction system which corrects for curvature of field and deflection introduced astigmatism (Figure 5). The deflection system is essentially similar to that in EBMI except that the working distance is increased and the number of turns on the deflection coils has been halved to increase the deflection amplifier bandwidth to 3 MHz.

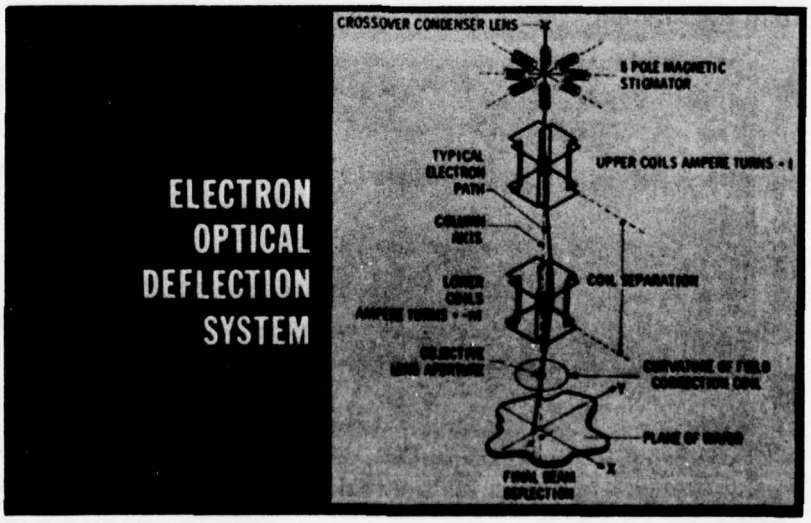


Figure 5. Electron Optical Deflection System

The pattern generating electronics of an e-beam writing system can be the limiting factor on cycle time rather than the resist sensitivity and the gun brightness. The pattern generating system developed for EBMI[3] and initially used in EBMIII has been redesigned and implemented in EBMIIIA. This has allowed proper generation of patterns at scanning speeds of 0.5 μm/μs and raster line spacings of 0.5 μm.

The electron-beam steering and error correction electronics in EBMIIIA is essentially similar to that in EBMI.[1] However, a new pattern generating concept has been implemented which allows greater speed, accuracy, and flexibility.

In general, the pattern figures are decomposed into general trapezoids in which the beam is scanned in a raster fashion parallel to the parallel sides of the trapezoid. Figure 6 shows the organization of the pattern generation section of the computer-electron beam interface. High speed is achieved by using a precision, wide bandwidth, free running sawtooth generator to generate the electrical signals for a first quadrant trapezoid. These signals are then routed through the "placement/view/fine adjust" circuitry which places and orients the geometry properly in the field. A basic time saving is achieved by using the free-running sawtooth generator because a real time digital-to-analog conversion at each scan end point is not required; sufficient data to write the entire geometry is obtained in one digital-to-analog conversion. This technique also allows greater precision in forming small geometries since it does not require the precise high speed matching and tracking of two 16-bit digital-to-analog converters (see Figure 7).

In addition to the speed increase, the added versatility of vector scan is available on an optional basis. This option allows the beam to be scanned at any angle relative to the coordinate axes.

4. Automatic Pattern Registration

Automatic pattern registration for slice printing is accomplished by scanning the electron beam across reference marks on the silicon wafer, detecting and amplifying the secondary and back scattered electrons, and processing this video signal to determine the correct position for the subsequently exposed pattern.

Problems which were initially considered using this approach[2] included: 1) the type of alignment mark, 2) the type of electron detector, 3) the method of processing the data acquired and, 4) the method of positioning the pattern.

Early development work on EBMI indicated that the combination of a reference mark etched in the silicon surface and a channel electron multiplier detector positioned near the wafer surface could provide the necessary bandwidth and signal-to-noise ratio. The small size of the channel

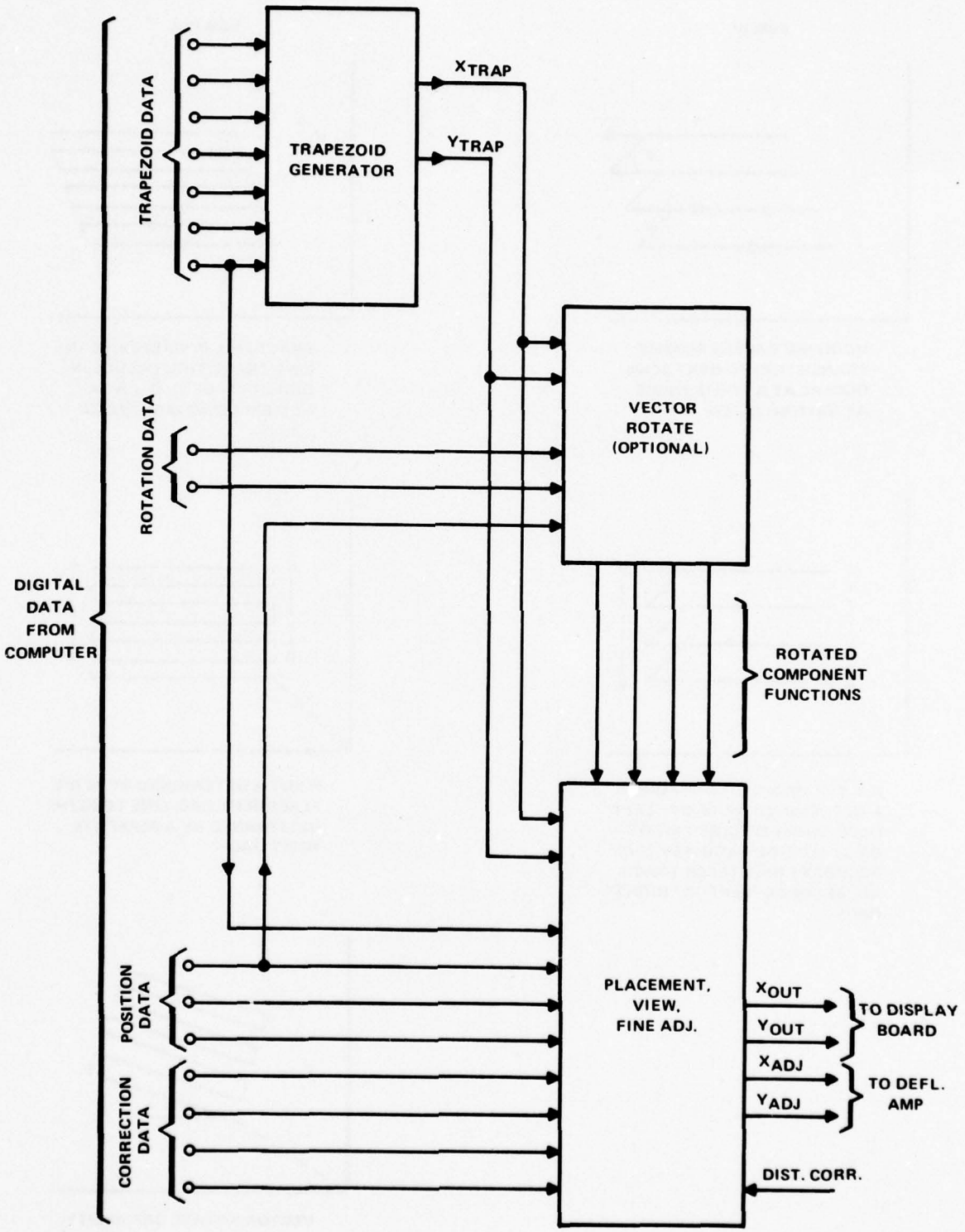
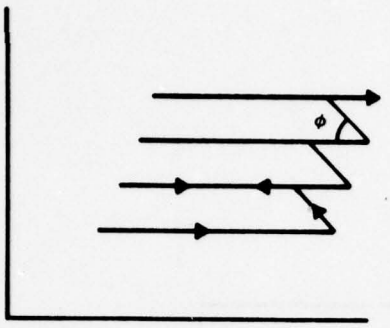


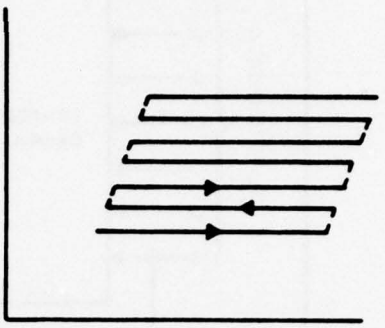
Figure 6. Computer-Electron Beam Interface

EBM III

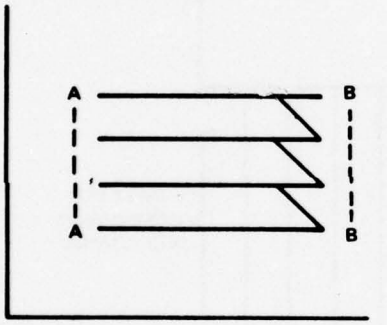


MODIFIED RASTER SCHEME. TRANSISTION TO NEXT SCAN OCCURS AT A FIXED ANGLE AT WRITING SPEED.

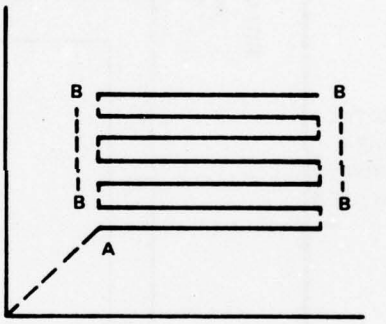
EBM IIIA



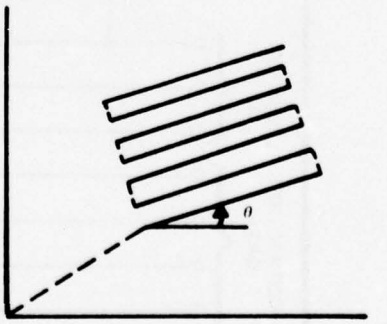
EXACT FILL-IN RASTER. SCAN LINE TRANSITION OCCURS IN DIRECTION OF SLANT AT A NON-EXPOSING HIGH SPEED.



X & Y COORDINATES OF POINTS A DETERMINED BY 16 BIT "LEFT" DACS, THOSE OF B, BY "RIGHT" DACS: METHOD REQUIRES VERY ACCURATE HIGH SPEED TRACKING BETWEEN "LEFT" & "RIGHT" DACS.



POINT A DETERMINED BY 16 BIT PLACEMENT DAC; LINE LENGTHS DETERMINED BY A SEPARATE 16 BIT DAC.



VECTOR ROTATE CAPABILITY.

Figure 7. EBMIII and EBMIIIA Raster Generation

multiplier enabled it to be located within 0.25 inch of the wafer and still maintain a short working distance and a large stage travel.

The signal obtained from scanning a silicon-etched marker is shown in Figure 8. The silicon-etched marker has the advantage of remaining on the wafer through all semiconductor processing so that it is not necessary to redefine additional markers for successive patterns. To obtain the necessary positional information, the video output is compared with a "video trigger-level" in a high-speed comparator to give a digital signal. This "video trigger-level" is a specific fraction (under operator control) of the peak signal level which is continuously measured by a peak level circuit.

To determine the X-coordinate position of a single L-shaped marker, the electron beam is scanned across the "vertical" limb of the marker 9 times. The technique is repeated on the "horizontal" limb to determine the Y-coordinate position. The scans are positioned along the markers at 3.2 μm intervals so that even if a portion of the marker is defective, accurate data can be obtained. The computer uses this data to calculate the position of the marker with respect to the scans and assigns a merit to the measurement based on the amount of deviation about the median position.

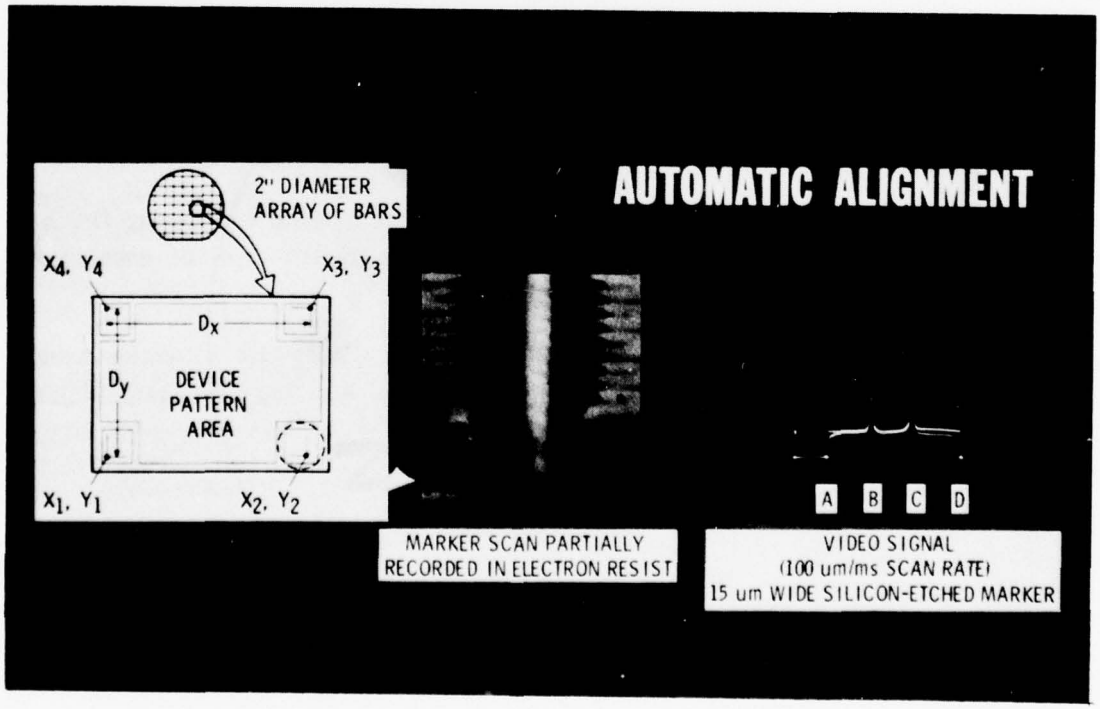


Figure 8. Automatic Alignment

The automatic pattern registration (APR) software program utilizes four L-shaped fiducial markers which can be positioned in any rectangular format in a field. The L-shaped markers are normally placed in the four corners of the field as illustrated in Figure 9. The APR program calculates the X, Y coordinates of these four fiducial markers by statistical analysis and determines the necessary corrections in X position, Y position, θ, X gain, Y gain, and orthogonality of the device pattern before exposure. The corrections are made in the following manner:

X and Y Shift – These corrections are made by software, the computer shifts all coordinates by a specific amount. The minimum shift increment possible on the 6.35 mm X 6.35 mm field is 0.125 μm.

X and Y Gain Adjustment – Hardware correction using multiplying DACs to form $x' = x + \lambda x$ and $y' = y + \mu y$ where λ and μ are digitally specific algebraic numbers. The minimum possible adjustment increment is 0.05 μm.

Rotation and Orthogonality Adjustment – Also a hardware correction using similar multiplying DACs to form $x' = x + \alpha y$ and $y' = y - \beta x$. The minimum possible adjustment increment is 0.05 μm.

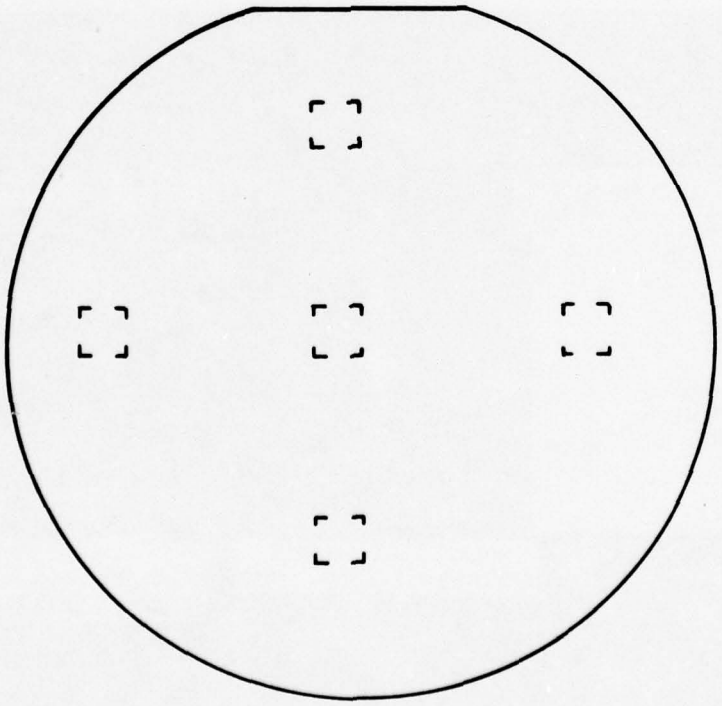


Figure 9. Alignment Markers

These adjustments are made with no movement of the wafer. The time taken by the machine to make such measurement of the four markers, carry out the statistical analysis and output the hardware adjustments is 27 ms. Typically two to three iterations of measurement and adjustment are required before the alignment is within the required accuracy. Testing the alignment accuracy of APR2 using a special vernier test pattern comprised of a 12 X 12 array of 0.060-inch square fields has shown 80% of the fields within ±0.2 μm. In fabrication of microwave transistors through four imaging levels on 0.060-inch square fields, alignment has been better than ±0.25 μm on 90% of the fields.

On the first phase Contract DAAB07-75-C-1297 special vernier tests showed that the automatic alignment system on EBMIII is capable of ±0.2 μm registration accuracy. Level-to-level registration on the six levels of the 256-bit CMOS RAM test cell showed equivalent results.

For photomask and large bar (>250 mils^2) fabrication, a commercial laser interferometer is used together with the automatic pattern registration system. The interferometer is utilized to determine the X and Y coordinate positions of the table (mask) and the e-beam APR2 system, described above, is used in combination with a special fiducial marker mask, fixed to the table and in the image plane, to determine X and Y gain, rotation and orthogonality. This procedure eliminates the problems with minor changes in accelerating voltage, lens current, deflection coil currents and focus over long periods of time. The X and Y positional measurement is closed loop, measured at each field, but X and Y gain rotation and orthogonality are only measured at the beginning of the generation of an entire mask. This technique does not require any type of fiducial marker for photomasks or one-level devices. Only one set of fiducial markers per wafer is required for slice printing.

Figures 10 and 11 show a schematic and a photograph of the mechanical portion of the pattern registration system (APR3) developed for EBMIII. The basic components are a 5525B Hewlett-Packard Laser Interferometer System (a helium-neon laser, two remote interferometers, and two beam detection units), a beam splitter, a beam bender, and two 6-inch chromium carbide reflecting surfaces mounted on the X-Y table.

Experience with the laser-controlled stage, the alignment accuracy on photomask pattern overlays and large wafer direct printing alignment has allowed us to refine the automatic alignment procedure for slices. In addition to be able to align on each bar as shown in Figure 8, a new method has been developed which requires 3-5 markers and combines the laser interferometer technique with the original technique. Termed "three-bar alignment", this method allows for both field and bar array correction, eliminates the problems with minor changes in electronics calibration, corrects for possible wafer distortion after processing steps, and allows a great savings in alignment time and silicon area used for alignment.

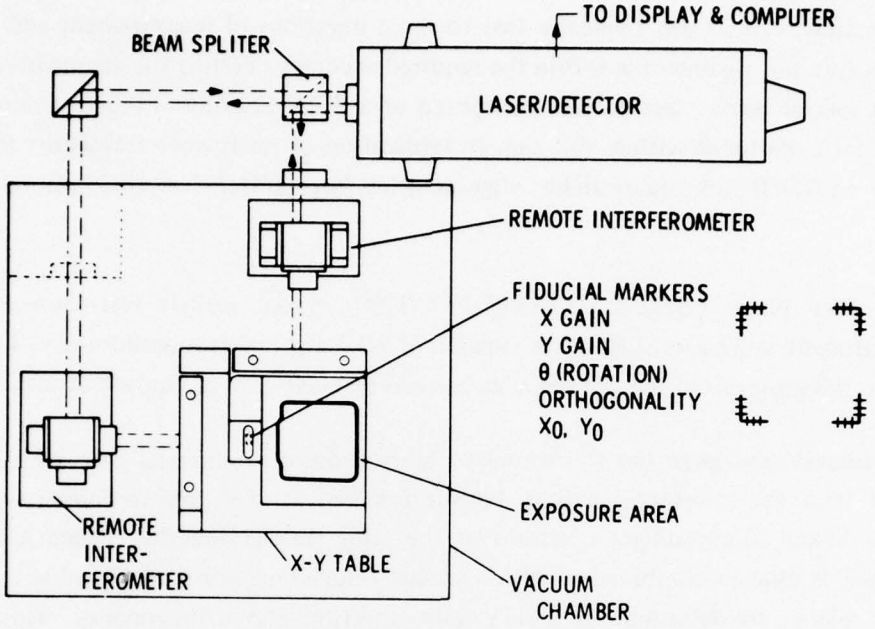


Figure 10. Pattern Registration System

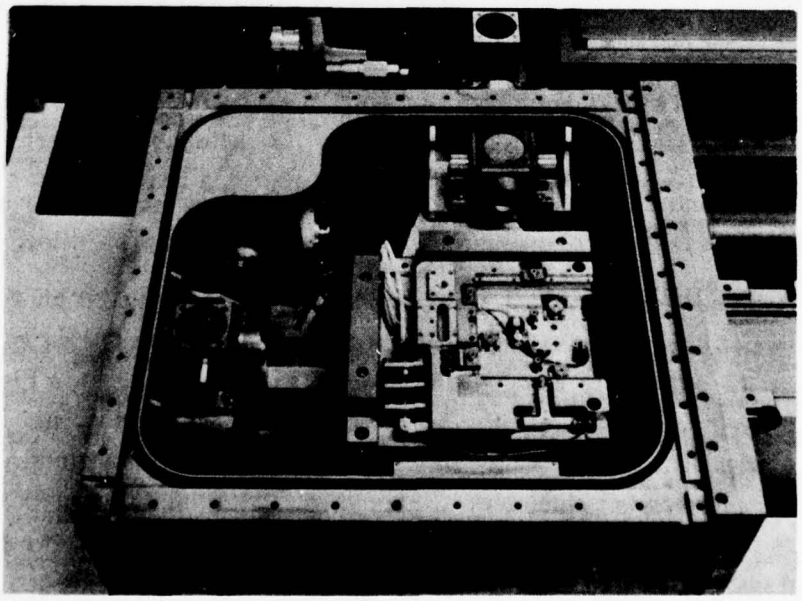


Figure 11. Laser Interferometer Controlled X-Y Table

As shown in Figure 9, five sets of alignment markers are printed on the wafer before the first patterning step. These markers are then etched into the silicon to serve as a constant reference for all subsequent patterning steps. This marker arrangement allows several schemes for slice alignment: quarter field, half field, or full field. In the quarter field alignment scheme, the auto align program drives the stage to within alignment range of each of the three sets of first quadrant alignment markers, and determines the position and bar shape as previously described. The marker position data of these three fields are then used by the laser controlled stage to correct the array gain and rotation. This feature corrects for any minor loading error in position and rotation of the slice in its holder. It also automatically corrects for linear distortions across the slice due to high temperature processing or clamping method and dimensional changes in the slice due to temperature. After this data is obtained and processed, the pattern is printed in the first quadrant.

The printing procedure is as follows: 1) Computer instructs stage to move to first bar location, 2) Stage moves to within ±1/2 step of location, 3) Laser interferometer determines exact actual location of stage and notifies computer, 4) Computer calculates position error and notifies stage shift correction circuit, 5) Stage shift correction circuit offsets beam deflection signal so that bar is placed properly, 6) Procedure is repeated for all subsequent bars. When the first quadrant is complete, the auto align and printing procedure is repeated until the slice is complete.

B. AUTOMATIC SLICE LOADING

1. Approach

The various constraints and requirements placed on an automatic slice handling system for an e-beam slice printing machine are:

1) Aligning the slice flat to within ±1/2°

2) Positioning the slice surface accurately in the focal plane of the beam

3) Reliable electrical contact to the backside of the slice

4) No mechanical vibration produced during slice exposure

5) 60 seconds or less vacuum cycle time

6) Compatibility with existing machine designs

The first three requirements are the most difficult to achieve. TI has been successful in the design, fabrication and implementation of an optical flat aligner capable of the required accuracy. Only a small amount of redesign of this existing prealigner is necessary to adapt it to the purpose described in this work.

The second requirement will be achieved by utilizing a "double banking" slice holder design in which the slice surface is first referenced to a surface inside the slice holder and the slice holder is then banked to a fixed reference plane inside the vacuum chamber.

Contact to the backside of the slice will be made via capacitive discharge forming circuit. A large capacitor is first charged with a power supply and then discharged through contacts to the backside of the slice to break down any SiO_2 present on the back of the slice. The contacts can then be tested via an ohmmeter circuit at any time during the exposure and can be reformed at any time if necessary. The contact points are part of the slice holder and contact forming and testing are done after final alignment and z-banking inside the exposed vacuum chamber. A prototype of this circuit has been built and tested and allows good reproducible contacts to be formed through 10,000Å SiO_2 layers.

Figure 12 is a drawing of the loading system. A cassette load of unexposed slices is placed in the unloader at point A. A single slice is unloaded and transported to point B and the flat located to within $\pm 1/2°$. The slice is then clamped into a slice holder, valve V_1 is opened and the holder is shuttled into the vacuum lock. The vacuum lock contains a 2-position elevator mechanism in which the loaded slice is elevated into position to be injected into position C. This elevation step places an empty slice holder in position D to be extracted from the lock to the prealign position B. Valve V_1 is closed and the vacuum lock is pumped to approximately 10^{-5} Torr; V_2 is opened and the slice

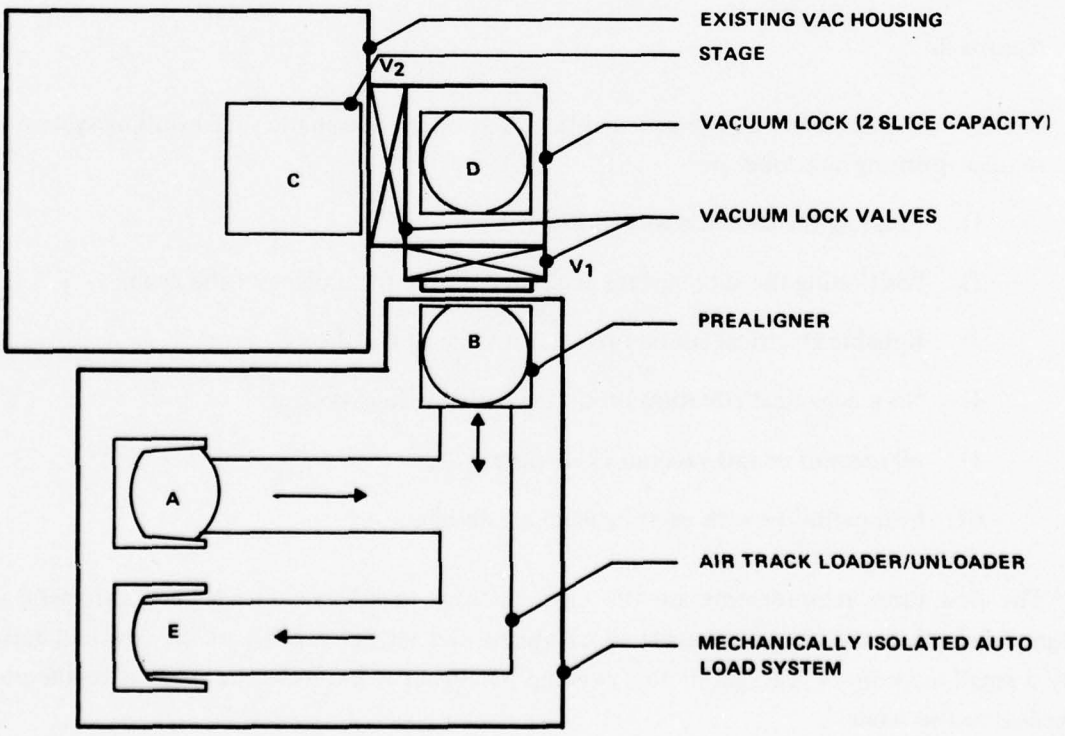


Figure 12. EBMIIIA Auto Load System

holder is placed at position C. V_2 is closed and the contacts are formed and tested and the slice exposure made. During this operation a second slice is transported to the prealign position B and the prealign and clamping are done in the second slice holder. This lock is vented with dry N_2 and V_1 opened and the second slice is placed in the elevator at D, V_1 is closed and the lock again pumped to $\approx 10^{-5}$ Torr. After the first slice is exposed, it and its holder are placed back into the elevator at D through V_2. The elevator then moves the second slice into position for placement at C. V_2 closes and the exposure sequence again begins. The lock is vented to atmosphere and the exposed slice and holder are pulled to position B. The exposed slice is removed and transported to E and a new slice is brought to the prealign position B and the entire sequence is repeated. In this way, an unexposed slice is always in the vacuum lock being outgassed by vacuum pumping while awaiting the completion of the exposure of the previous slice. Continuous slice flow is maintained and nearly all overhead time associated with slice transport and vacuum cycling is eliminated.

C. FUNDAMENTAL CHEMISTRY OF ELECTRON RESISTS

As a high-energy electron penetrates a layer of resist, it undergoes elastic and inelastic collisions with the polymer molecules. The inelastic collisions transfer energy to the polymer. The more numerous elastic collision has no known effect on the molecules. Although the initial form of the energy absorbed is not known, one of the final effects is chemical reaction. The two reactions which lead to patternable images are chain decomposition and cross-linking. If chain decomposition predominates, the polymer will behave as a positive resist. If cross-linking predominates, the polymer will behave as a negative resist.

1. Positive Resists

When a polymer undergoes random chain scission, one or more of several reactions may occur:

1) $P^*_n \rightarrow P^*_{(n-m)} + P^*_{(m)}$

2) $P^*_{(n-m)}$ [or P^*_m] $\rightarrow PP_{(n-m-a)} + aM$

3) $P^*_{(m)}$ [or P^*_{n-m}] $\rightarrow P^*_f + f$

4) $P^*_{(n-m)} \rightarrow P_{(n-m)}$

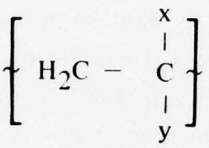
5) $P^*_{(m)} \rightarrow P_{(m)}$

6) $P^*_{(n-m)} + P^*_{(m)} \rightarrow P_n$

7) P^*_m [or $P^*_{(n-m)}$] $+ P_n$ (or P^*_n) $\rightarrow P_{n+m}$

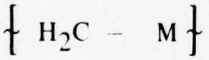
In these reactions, P is polymer, * represents an unstable state, M is monomer, f is low molecular weight fragment, PP is low molecular weight polymer, n and m are the degrees of polymerization of the polymer, and a is the number of moles of monomer lost in the reaction. This mechanism does not list all the reactions that can take place, but only those yielding resist images. With this abbreviated scheme, it is obvious there are many competitive reactions. Reactions 1 and 2 result in the polymer performing as a positive resist. The other equations negate these two reactions. The mechanism determines that the random fragmented polymer must unzip, or decompose, rapidly. The unzipping is a depolymerization which yields large amounts of monomer from which the polymer was orginally made. Most polymers do not decompose when cleaved in the solid state because the two fragments cannot migrate away from each other and are likely to combine and reform the original polymer units.

There are two distinct polymer types known to decompose faster than they recombine in the solid state. The first polymer is the alpha substituted polymer.[4]



(I)

where x and y are groups other than hydrogen. The second type contains volatile molecules in the polymer backbone:



(II)

where M is a valence-satisfied molecule. Perhaps the best example of structure I is polymethylmethacrylate (PMMA). It was the first positive e-beam resist and is the most widely used. Although PMMA meets almost every resist requirement, it, unfortunately is not fast enough. However, with other substituents, faster type I polymers can be made. Polymers with structure II are best represented by the olefin-sulfone polymers of which polybutene sulfone (PBS) is the most widely used.[5] PBS is the fastest known positive resist reported to date. The sensitivity of PBS is in the range suitable for economical bipolar 256-bit RAM fabrication.

In addition to these two polymer structures, there is a third circumstance that can cause polymers to decompose. If a polymer is irradiated above its ceiling temperature, depolymerization is enhanced. The ceiling temperature is that temperature at which the free radical catalyzed polymerization will not take place because the depolymerization reaction rate is as fast as the

4. Chapiro, A., "Radiation Chemistry of Polymeric System," *Interscience Publisher*, New York (1962).

5. Thompson, L. F. and Bowden, M. J., "A New Family of Positive Electron Beam Resists," *J. Electrochem. Soc.*, **120**, 1723 (1973).

polymerization rate. This temperature rate enhancement of positive resists is important since the biggest drawback to positive resists is their sensitivity.

The sensitivity of a positive resist is a combination of the radiation scission yield and development conditions. The fact that the scission yield (G_s) does not determine the resist speed is demonstrated with the celluloses.[6] These polymers have a G_s about five times greater than PMMA, yet, their resist speed is about five times slower. The importance of the proper developer is easily illustrated with any positive resist. For example, PBS developed with isobutylmethylketone is three to four times faster than when developed with a butylacetate alcohol mixture. Yet, both solvents yield good images.

2. Negative Resists

The most common reaction for a polymer in the solid state to undergo upon high-energy irradiation is cross-linking. Cross-linking forms an insoluble molecular network which is the basis of negative resists. One reaction pathway to cross-linking was shown in reaction 7; however, there are many others. Any polymer, activated through bond cleavage, may react with another activated or inactivated polymer resulting in a cross-link. A chain reaction may also ensue in which each cross-link reaction causes the formation of a new activated species. This reaction can lead to very high yields and is probably one of the main reasons negative resists are much more sensitive than positive resists.[6]

As with positive resists, the chemical structure of the polymer is a primary factor in determining the sensitivity of negative resists. Polymers containing olefin, epoxy, and vinylsiloxane groups are from ten to 100 times more sensitive to electron bombardment than polymers without these groups.[6] Variations of structure within these three groups are also important.[7] Molecular chains that contain olefin groups in the backbone (III) are less sensitive than those with vinyl groups (IV):

$$\left\{ CH_2 - \overset{H}{C} = \overset{H}{C} - CH_2 \right\} \quad \text{(III)}$$

$$\left\{ H_2C - \underset{\underset{\underset{CH_2}{\|}}{CH}}{\overset{|}{CH}} \right\} \quad \text{(IV)}$$

6. Brewer, T. L., "Electron Beam Resists," *Society of Plastic Engineers,* Technical Conference on Photopolymers, 138 (October 1973).

7. Brewer, T. L., "High Speed Electron Resists," Electochemical Society National Meeting, San Francisco, California (May 1974).

The sensitivity of a negative resist is also affected by the molecular weight of the polymer. Experimental studies have shown that up to molecular weights of about 100,000 there is a linear increase in resist sensitivity with molecular weight. Above that, the increase becomes nonlinear.[6] The nonlinearity is probably due to the polymer molecules reacting with themselves; although no direct evidence is available.

Unlike positive resists, the developer has very little effect on the sensitivity of negative resists. However, it is important in determining the image quality.

The contrast of a resist also is one of the main factors affecting image quality. In general, negative resists have lower contrasts than positive resists, and therefore poorer images.[7] The contrast can be controlled to some extent by two experimental variables. The polydispersity of a polymer is the measure of the range of molecular chain lengths in a polymer. Polymers with low polydispersities (narrow range of chain lengths) have better (higher) contrasts as resists.

The second variable that controls contrast is the competition between scission and cross-linking.[7] Most negative resists undergo some decomposition as well as cross-linking when exposed to high-energy electrons. As the decomposition yield increases, the contrast (and the sensitivity) decreases.

Considered together, these facts indicate that a negative resist should contain either olefin, epoxy, or vinyl siloxane groups, have a narrow polydispersity, and should not contain weak bonds in the polymer backbone that will promote decomposition.

Table II lists several types of electron resist materials and their relative sensitivities.

D. ELECTRON RESIST PROCESS DEVELOPMENT

A program to implement high-speed resist technology into device fabrication can be successful if the resist chemistry and processing parameters are dependently developed. The resist chemistry determines the main fundamental properties such as sensitivity, resolution power, plasma stability, coating performance, and solubility. The processing parameters are used to fine tune the resist toward a specific device application. Adjusting these parameters will help control undercut, pinholes, opaque spots, and geometry size.

A substantial quantity of resist chemistry and processing data has been amassed. This now allows the device fabricator to choose one or more of several resists for the particular device manufactured. A list of the resists currently available for device fabrication at Texas Instruments is

Table II. Types of Electron Resist Materials

Polymer	Relative Sensitivity	Type*
Polymethylmethacrylate	1	P
Polystyrene (M.W. 97,000)	.4	N
Polystyrene (M.W. 33,000)	.12	N
Negative Photoresists	25	N
Chlorinated Polyethylene	25	N
Diene Polymers	10-100	N
Vinylchloride Copolymers	5	N
Monomeric Epoxide	1	N
Epoxidized Polymers	100+	N
Polydimethylsiloxane	1	N
Polyvinylsiloxanes	100	N
Kel-F	3	N
Poly (isobutenylmethyl ketone)	.1	N
Polycaprolactone	.3	N
Polyorthodiallylphthalate	10	N
Fluoropolymers	80	N
Cellulose Acetate	.2	P
Cellulose Triacetate	.2	P
Cellulose Acetate Phthalate	.2	P
Polyacetal	.5	P
Polymethylstyrene	.5	P
Polyisobutylene	1	P
Vinylester Polymer	8	P
Olefin Sulfone Polymers	10	P
Acrylonitrile Polymers	10	P

P = Positive

N = Negative

Table III. Resist Sensitivities

Resist	Type	Sensitivity ($\frac{\text{Coulombs}}{\text{cm}^2}$)
TI309	Neg	1.3×10^{-6}
TI313	Pos	3.5×10^{-6}
TI333	Pos	1.5×10^{-5}
Bell PBS[5]	Pos	1.3×10^{-6}
Bell PGMA[8]	Neg	2.5×10^{-7}
PMMA	Pos	5×10^{-5}
Polystyrene	Neg	7.9×10^{-5}

Table IV. Resist Developers

Resist	Developers
TI309	Xylene
	Toluene
	Cyclohexanone
TI313	Cellosolve solvents
	$C_6 - C_9$ ketones
	Esters
Bell PBS	Methyl isobutyl ketone
	5 methyl – 2 hexanone
PMMA	Isobutyl methyl ketone/isopropyl alcohol 1/3
	Isobutyl methyl ketone
	Ethanol
Polystyrene	Xylene
	Toluene

shown in Table III. Many of these resists have already been used for specific device fabrication. These resists offer a wide range of exposures, contrasts, etching techniques, and image phase (negative or positive). Several chemical developers are also available for these resists, as shown in Table IV.

8. Thompson, L. F. and Feit, E. D., "Organic Coatings and Plastics," *Preprints*, Chicago ACS Meeting, April 1973.

In order to develop the resist chemistry and interdependent processes for a particular device, such as the 256-bit bipolar RAM, there is a series of well-defined parameters that must be characterized and optimized. Basically these parameters are:

1) Exposure characteristics of the resists.

2) Adhesion to the specific surfaces involved in making the device.

3) Etch resistance with both wet and dry processes.

4) Ion implantation masking ability.

5) Resist removal and clean up compatible with the device and its chemical composition.

Precise control and implementation of each one of these five areas is necessary for the successful fabrication of a microcircuit.

In order to understand the problems associated with making a new microcircuit, it is important to have a conceptual view of these five parameters.

Exposure Characterizations

Characterizing the exposure involves determining how fast a particular pattern can be written, the minimum line widths and spaces that are obtainable, and the dimensional control of the pattern. In particular, this last point deals with the changes in pattern size that occur with different doses and different resist thicknesses. Both of these parameters must be adjusted to keep the pattern sizes within specific tolerances. Therefore, curves must be obtained that relate.

1) Spin speed to thickness.

2) Thickness to dimensional changes.

3) Line width to dose.

4) Line quality to a dose.

5) Dose to dimensional changes.

6) Minimum and maximum exposure dosage.

Unfortunately, one resist will not be optimum in all areas. Therefore, the resist used will be dependent upon the specific device level. The minimum geometries, spacing and pattern density (writing time) of the level will dictate the exposure characteristics needed. Image phase (i.e., negative acting or positive acting) of the resist is also an exposure characteristic that is dependent on the above device level requirements.

Adhesion

Whether a resist adheres to a surface or not determines its usefulness as an etch mask. Every surface used in making a device must be checked for resist adhesion. For example, with bipolar devices, resist adhesion to silicon, silicon dioxide, boron doped silicon dioxide, phosphorous doped silicon dioxide, aluminum, and aluminum oxides must be checked. Each of these surfaces presents a unique problem with resist adherence. Initially, data on the smallest line width that will adhere after development and the amount of undercut upon etching must be obtained. Only rarely is poor adhesion noted during the development step. Poor adhesion at this step usually indicates a contaminated surface or resist. Adhesion loss more often occurs during etching. In fact, it is very difficult to separate adhesion problems and etching processes. If problems exist, then adhesion promoters have to be investigated through the etch steps. Also, if several different etchants are available for the same material, adhesion should be investigated for each one.

Etch Resistance

The resistance of the electron resist to each etchant used in the device process (under the conditions used) must be determined. The two things that must be investigated are whether the polymer reacts with the etchants and whether the etchant is capable of displacing the polymer from the surface of the slice.

Some of the common wet etchants that might be used with the bipolar devices include 10% HF, buffered HF, HF-HNO_3, H_3PO_4, and KOH. Many of these are available commercially under such names as Bell-2 and common oxide etch. Fortunately most resists can withstand the strong acids under the conditions normally used. However, in some cases the resist must withstand the etch at elevated temperatures (above room temperature) for relatively long times (>10 minutes). The necessity of such conditions is one of the most difficult hurdles in process development. Also, most resists show a loss of adhesion when put in strong bases for extended periods.

In terms of dry etch processing, the main concern is whether the resist etch rate is sufficiently slower than the substrate etch rate. The two main dry etch techniques used are plasma and ion milling.

Plasma etching is based on the formation of a high-energy chemically active species that can react with the substrate to form a volatile compound. It is commonly used in the etching of silicon nitride, silicon, tantalum, and chromium. It is generally not used on aluminum or gold. The chemically active species commonly used in these etchants are fluorine, oxygen, chlorine, and nitrogen. Unfortunately, these species also attack the resist material. There is some variance in the resist etch rate with different etchants and resists. Thus the resist etch rate must be measured for each plasma process used. Qualitatively resists etch faster in oxygen-rich plasmas and slower in

fluorine plasmas. Also positive resists etch faster than negative resists and therefore, thicker films of positive resists must be used.

Ion milling is not as chemically selective as plasma etching. In principle, a substrate is bombarded with high-energy ions (usually argon) that literally knock the substrate molecules out of the surface. This nonselectivity means that the resist will etch at about the same rate as the substrate, thereby requiring resist thicknesses comparable to that of the substrate.

Different materials do have different milling rates. The technique is most commonly used for gold since its rate is higher than that of the resist. However, ion milling has been used for a large number of different substances including chromium, aluminum, and silicon where the rates are similar to that of the resist. As with plasmas, positive resists ion mill faster than negative resists. For that reason, a negative resist is preferable in a device-level requiring ion milling.

One reason for the lower susceptibility of negative resists to the dry process is their efficient mechanism for cross-linking. The greater the amount of cross-linking, the more resistant the resist is to erosion. The increased cross-linking can come from increased exposure, higher bake temperatures, or from the dry process itself.

Ion Implantation

The use of ion implantation adds a whole new set of problems for resists. This is due to the facts that very thick films (>5000 Å) of resist must be used and the implantation process uses very high energy particles (>1 kV). The thick films cause problems because it is very difficult to obtain small geometries (<2 μm) with films over 8000 Å thick when e-beam exposure is used. This is due to the backscattering of the irradiating electrons. The second problem results from the fact that it is very difficult for polymers to withstand the high energy ions. The problem is primarily manifested in positive e-beam resists, since they are designed to decompose upon high energy particle bombardment.

The ion implantation blocking ability will have to be measured for each resist and each dopant. This is because the blocking ability of a resist will vary with film density, film thickness, percent film decomposition under ion bombardment, size of the dopant atom, and dopant accelerating voltage. The blocking capabilities of most of the resists mentioned previously are not known. Data has been gathered for polystyrene and polymethylmethacrylate. However, the relative effectiveness of negative versus positive resists has not yet been demonstrated.

Resist Removal and Clean-up

This somewhat mundane step is one of the most critical. If the surface is not completely cleaned after each level, there is no way that the next level can be successfully completed. Any clean-up acid residue, resist, or etchant residue left on the surface will result in poor adhesion for the next layers. The surfaces must be rinsed thoroughly and spot checked for contamination. These spot checks involve both visual inspection and analytical inspection involving such techniques as Auger and X-ray microprobe spectroscopy.

It is also important that the clean-up process not be so harsh as to affect the device levels already completed. This can be a real problem with negative e-beam resists since they are very difficult to remove after exposure. Often, unusual chemical mixtures and/or plasma must be resorted to, since common cleaners such as J-100 do not do a thorough job of resist removal.

The above discussion was designed to point out the general importance of each of the five steps by giving a few specific examples of *foreseeable* problems (i.e., a conceptual view). It is important to note the interdependence of all of these steps. This means it is almost impossible to define final processes by optimizing each step. Each step demands a comprise from all the others. Therefore, the approach must be to gain as much quantitative information on each step as possible and then attempt to fit it together to make a process.

E. SCHOTTKY BIPOLAR RAM PROCESSING

1. Introduction

There are many possible bipolar processes that could be used in conjunction with e-beam pattern definition to build memory devices. Among those are dielectric isolation, isoplanar, double level metal, etc. While all of these processes have merit, the process chosen for this program will be the junction isolation Schottky process which is used by Texas Instruments in building the 54S/74S series of products.

2. Process Description

The process to be used is outlined in Table V and Figure 13. Some procedures such as clean-ups and etches are omitted from the table but of course are used and are typical of good production practice.

3. Resist and Etching Selection

Except for metallization, the patterning steps shown above involve etching between 2000 Å and 10,000 Å of SiO_2. Because plasma etch rates of SiO_2 are low and resist lifetimes are limited in the plasma environment, we intend to etch SiO_2 using common buffered HF solutions. Our requirements for electron resists are thus dominated by two factors: 1) Sensitivity ($\geq 2.5\ \mu C/cm^2$) and 2) good adhesion to SiO_2 for wet chemical etching. Among the resists that we have investigated whose sensitivities are greater than $2.5\ \mu C/cm^2$, we have demonstrated good oxide patterning capability with polybutene sulfone (PBS) resist. Further, PBS, being a positive resist, leads to advantages in minimizing area scanned and increasing throughput for most of the pattern levels.

Table V. Schottky Bipolar RAM Process

1) Substrate
2) Initial Oxidation
3) DUF* oxide removal
4) DUF* deposition
5) DUF* drive
6) Strip oxide
7) Epitaxial layer
8) Second oxidation
9) Isolation oxide removal
10) Isolation deposition
11) Isolation drive
12) Base oxide removal
13) Base deposition
14) Base drive
15) Emitter oxide removal
16) Emitter deposition and drive
17) Contact oxide removal
18) Platinum deposition
19) Alloy platinum
20) Ti-W, Aluminum deposition
21) Metal removal
22) Sinter metal

*Diffusion Under Film – Buried Layer

Metallization for the 256-bit RAM will be Ti/W/Al which we expect to define by plasma etching. PBS cannot be used as a plasma etch mask and there are no other high-speed positive resists available. We will therefore use the negative resist TI309, which has a sensitivity of $\sim 2.5\ \mu C/cm^2$. Some experimental results have been completed which show that Al can be plasma etched using TI309 as a mask. If difficulty arises in plasma etching Al, alternative wet chemical etchants which we have developed for use with TI309 can be substituted. (See Figure 14).

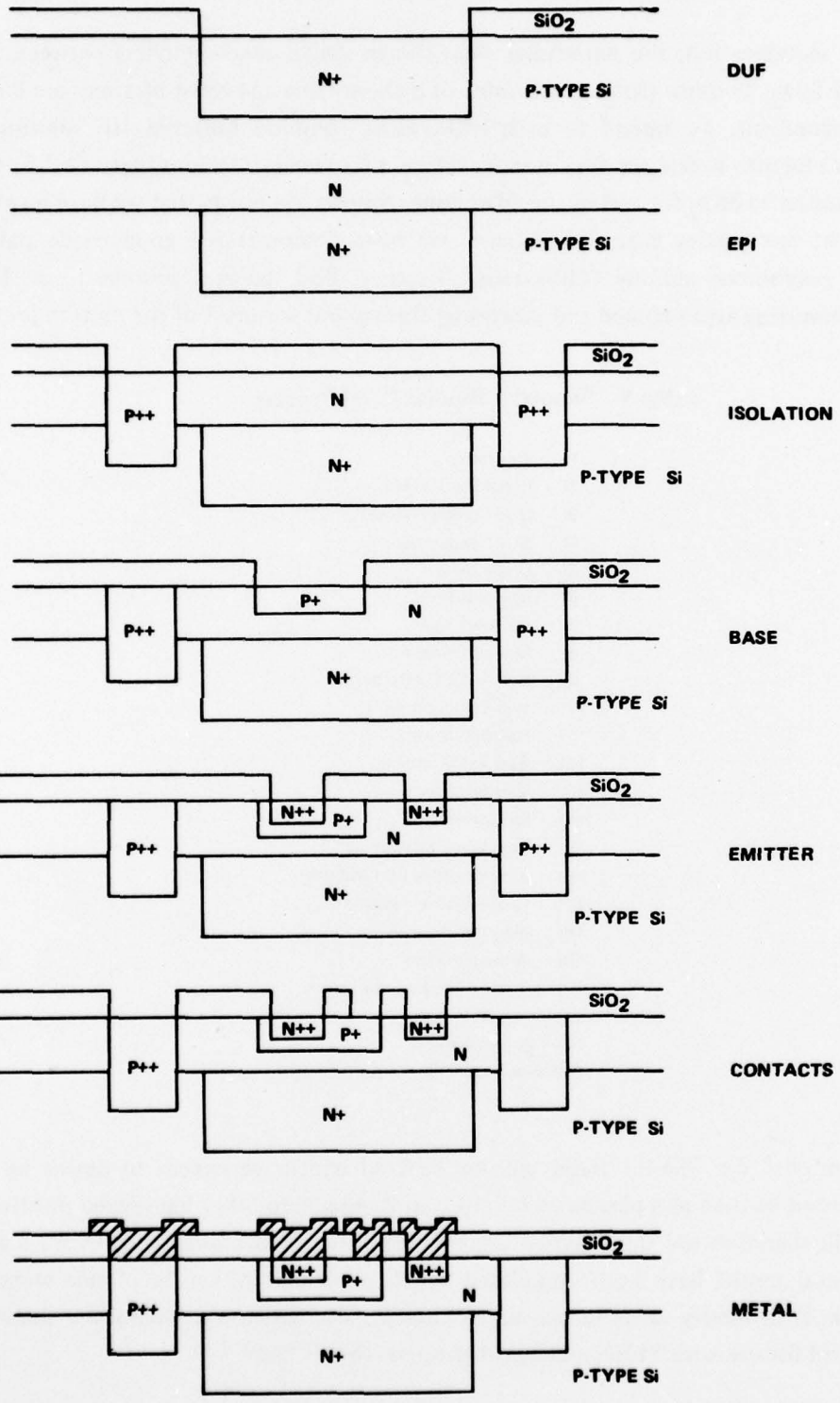
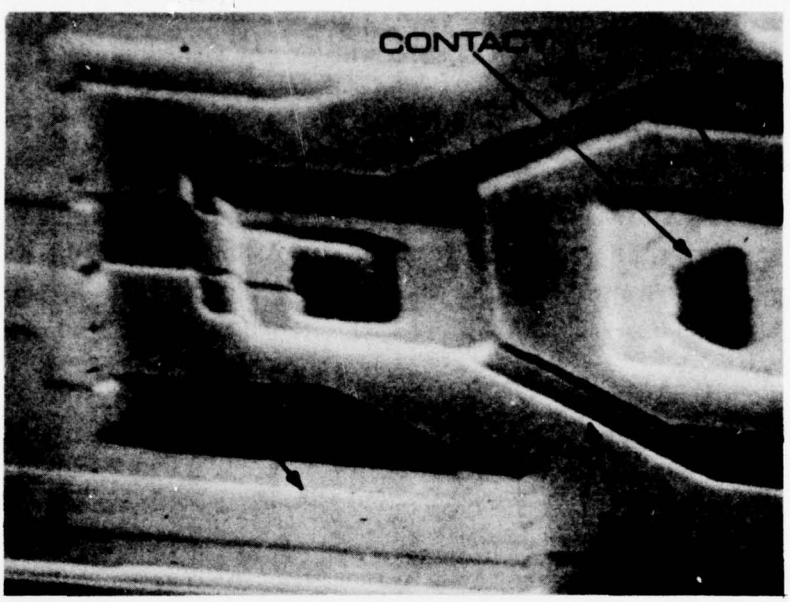
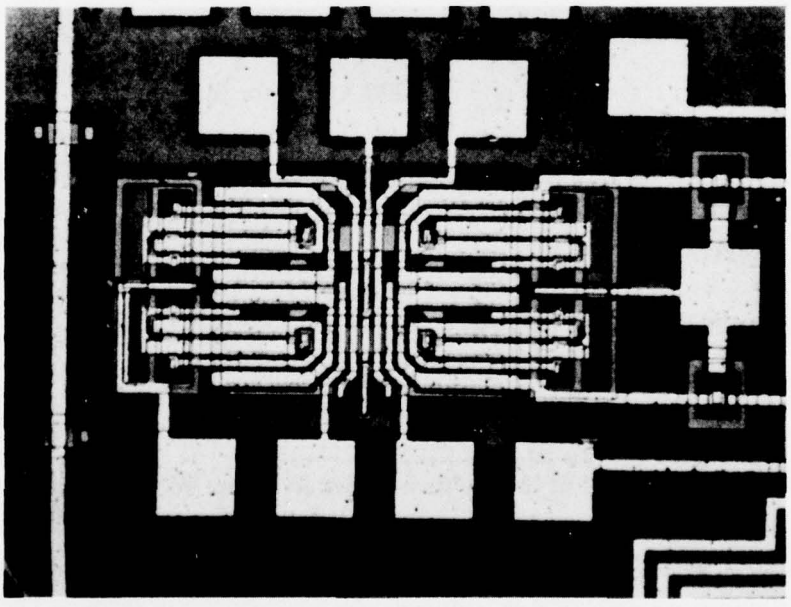


Figure 13. Sectional View of Slice at Various Process Steps



a. CMOS RAM MEMORY CELL AFTER CONTACT OR USING PBS ELECTRON RESIST



b. FOUR CMOS RAM CELLS (15.1 MIL^2) AFTER METAL (AL) DELINEATION USING TI-309 ELECTRON RESIST AND WET ETCHING

Figure 14. E-Beam Defined Geometries with PBS and TI309

Resist processing will be done on completely automated, cassette loaded spin coaters and developers. This will provide maximum throughput and reproducibility while minimizing slice handling. These machines are installed in a horizontal laminar flow clean room to minimize particulate contamination. Wet chemical processing will be performed in vertical laminar flow clean hoods installed in this same room.

The feasibility of IR baking for electron resist processing will be demonstrated. Cassette loaded ovens with belt drive through three temperature zones and nitrogen air curtains will be used. The wafers will load individually onto the belt and face the IR emitters directly.

4. Alignment Marker Processing

As mentioned above, e-beam alignment markers are features etched 2-4 μm deep in the silicon substrate. We expect to fabricate these markers using shielded plasma etching in one of two possible processing schemes: 1) the bare silicon slices will be coated with PMMA resist, marker patterns will be exposed, markers plasma etched and resist plasma stripped. The first oxide will then be grown and the DUF level will be patterned in PBS with alignment to the previously etched markers. 2) In the second scheme the alignment marker pattern will be included with the DUF pattern and etched into the first oxide using PBS resist. The slices will then be coated with PMMA to protect pattern areas while windows are opened around the alignment masks. The alignment masks will then be plasma etched using the oxide as a mask.

We expect to use a plasma etch rate of 2000 Å/min for Si; under the same conditions using shielded plasma etching, SiO_2 has an etch rate of 200 Å/min while PMMA has an erosion rate of about 150 Å/min. Thus we will easily be able to etch deep into the silicon. The exact depth, width and edge profile of the markers will be somewhat determined by the kind of coverage obtained in depositing the epi layer.

F. SCHOTTKY BIPOLAR RAM DESIGN

1. Inputs

The circuit schematic for all of the inputs is shown in Figure 15. This circuitry was designed to give very low high- and low-level input currents and very high performance. The low input currents allow higher fan-out capability in an entire memory system. The use of Schottky diodes and transistors in the inputs increases the performance over non-Schottky devices. The inputs also have clamp diodes to protect the circuitry if the input voltage should go negative.

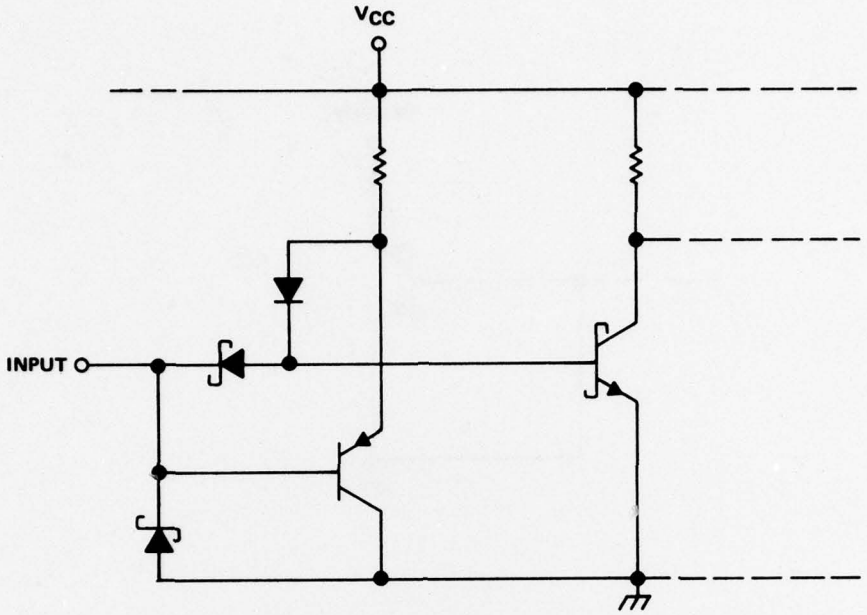


Figure 15. Input Circuitry

2. Output

The circuit schematic for the output is shown in Figure 16. The open-collector output permits connection of one or, for larger word capacities, a number of outputs to a common bus through a single pull-up termination.

3. Memory Cell

The circuit schematic for the memory cell is shown in Figure 17. The cell is basically two cross-coupled inverters and two sense transistors. Information is written into the cell or read from the cell along the sense lines. The cell is enabled or disabled using the address line. When the address line is high information can be read from or written into the cell. When the address line is in a low state the cell is disabled and no information can be read or written.

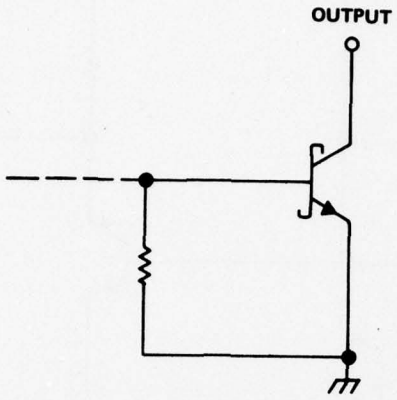


Figure 16. Output Circuitry

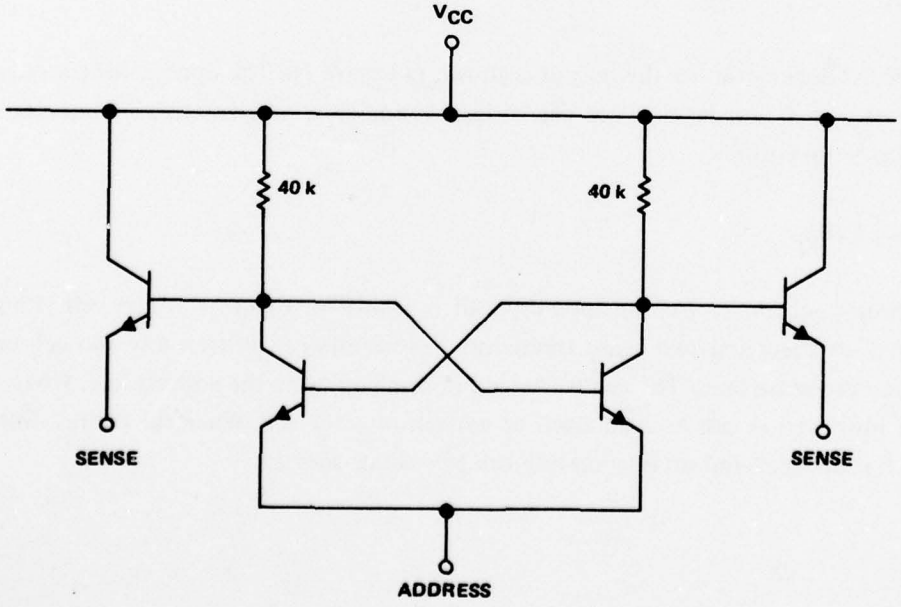


Figure 17. Memory Cell

4. System Design

The proposed IC is a single monolithic integrated circuit containing a 256-word by 1-bit fully static random access non-destructive readout memory. The memory if fully decoded requires only 8 address lines to select one of 256 storage locations. An additional line, write enable, is provided to enable the memory to modify the stored data. Separate Data Input and Data Output lines are provided for minimum interaction between input and output functions. Three chip enable lines are provided to simplify the decoding required to achieve the desired system.

The basic logic diagram is shown in Figure 18. The memory matrix is organized in an array of 16 rows and 16 columns. The address inputs A, B, C and H go to a 4-to-16 line decoder and determine the memory column selected. The address inputs D, E, F and G go to a 4-to-16 line decoder and determine the memory row selected. The logical operational mode (truth table) is shown in Table VI.

5. Terminal Connections

The terminal connections for the 256-bit RAM are shown in Figure 19.

G. ELECTRICAL TESTING

Electrical testing for the 256-bit RAM will be accomplished using existing automatic test systems at Texas Instruments. The basic equipment proposed for the test is the High Speed Measurement (HSM) System and the Numerical Exerciser for Memories (NEM).

Table VI. Logical Operational Mode

Function	Inputs		Output
	Chip Enable†	Read/Write	
Write (Store Complement of Data)	L	L	H
Read	L	L	Stored Data
Inhibit	H	X	H

H = high level, L = low level, X = irrelevant

†For chip-enable: L = all $\overline{CE}$ inputs low

H = one or more $\overline{CE}$ inputs High

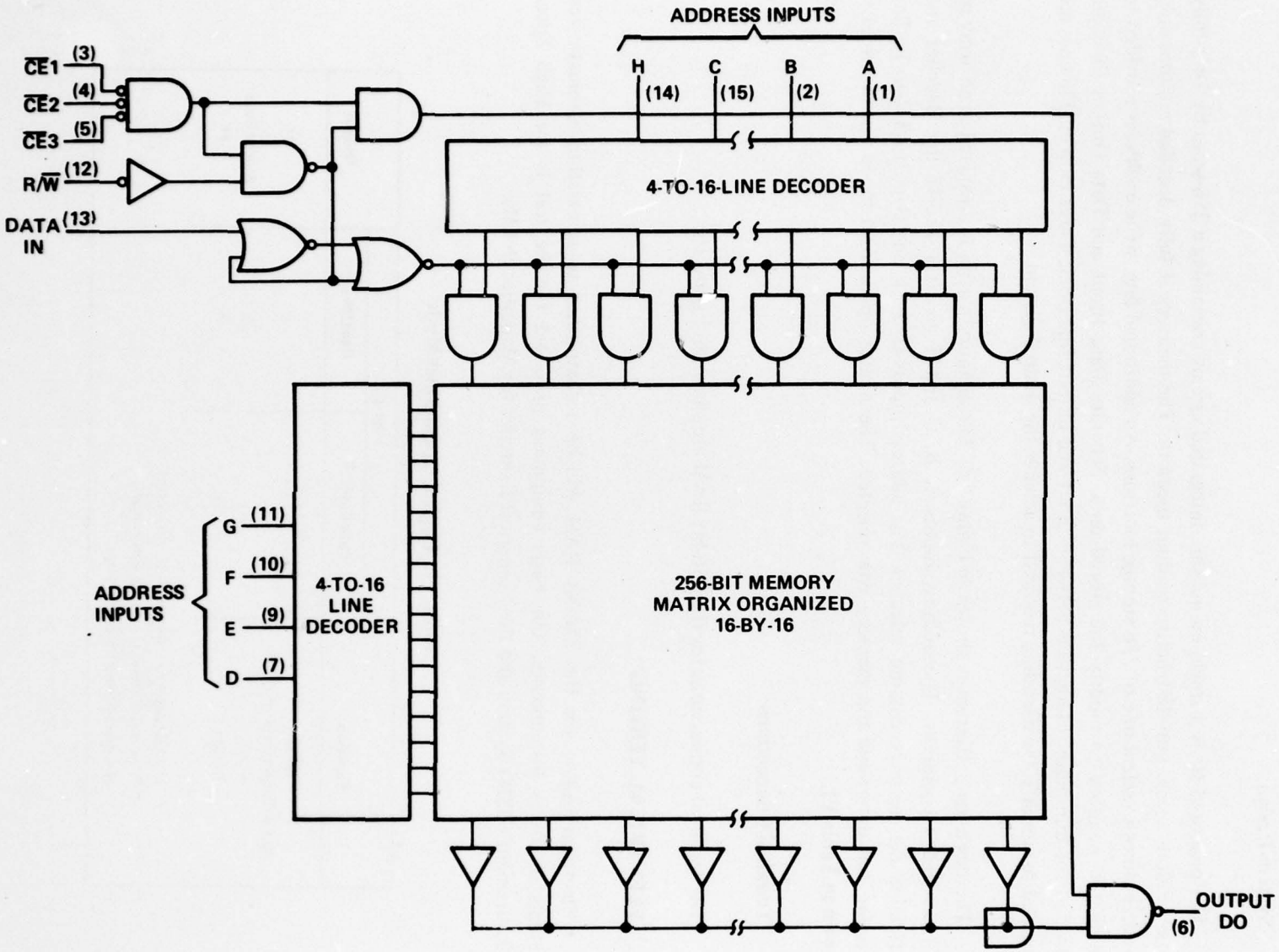


Figure 18. Logic Diagram

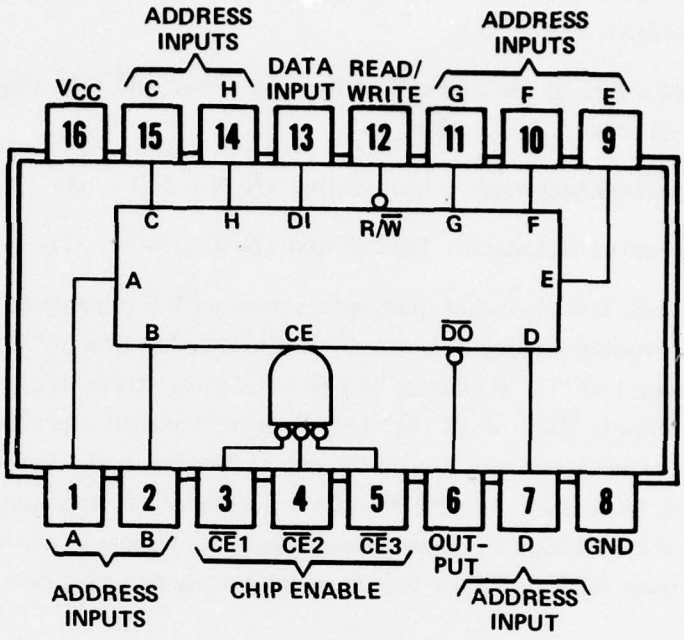


Figure 19. Terminal Connections

The HSM will be used to test the memories while they are in slice form. It will perform all the dc tests such as I_{CC}, V_{OL}, I_{OH}, etc. and will also do functional testing on the memory cells and peripheral circuitry.

The NEM will be used to test the memories after they have been packaged. Programming of the NEM is accomplished with a RAM memory supplying instructions for support as well as test instructions to implement exercise algorithms. Some of the algorithms presently in the software library are as follows:

1) (a) Write a zero in each device location (1, 2, 3 . . . N)

   (b) Read and verify a zero in each location (1, 2, 3 . . . N)

   (c) Write a one in each device location (1, 2, 3 . . . N)

   (d) Read and verify a one in each location (1, 2, 3 . . . N)

2) (a) Read a one in first cell, write back a zero, and read a zero. Repeat process for all cells (1, 2, 3 . . . N)

(b) Read a zero in the first cell, write back a one; and read a one. Repeat process for all cells (1, 2, 3 . . . N)

(c) Repeat (a) backwards – last cell first. (N, N-1, N-2 . . . 1)

(d) Repeat (b) backwards – last cell first. (N, N-1, N-2 . . . 1)

3) Access 0-1-0: This algorithm starts with a memory full of zeros and a 1 in location 0. Begin by reading a background of "0", a reference location of "1" and again reading a background of "0". Repeating this process, thus, verifies the access time (address to data output) "both ways" between location 0 and all other locations, 1 through N: then writes a one into location 1 and verifies its access time with respect to all remaining locations 2 through N; then reiterates this process until a one is written into the final location N, whose access times with respect to all other locations have already been verified. Notice that data out complements for both directions of read access.

4) Access 1-0-1: This test initializes the device to all ones, then tests individual access times by using the same general procedures as in test 3 above except that all data zero/one references are reversed. This time the data output transitions for each read cycle are 1-0-1.

5) Random data pattern: This test will generate a 10 Bit MLS pseudo random data sequence for writing into and reading from the device under test. The sequence repeats after 1023 memory cycles. This pattern will be displaced by one bit prior to each write all, read all such that after n loops, the random pattern will have been rotated completely through memory.

6) Walking Disturb: This is the most thorough single test of all present algorithms. It is a combination of the "walking ones and zeros", access time verify to and from every location and, address to write enable set-up check to and from every memory address. With the exception of memory enable/exercise, it will do an equal to or better than evaluation of any failure mode exercised by all the preceding algorithms. However, it does have a limitation; execution time.

The NEM system is designed such that generating new algorithms is almost limited to one's own imagination.

All of the final functional dc and ac testing will be performed on the NEM. The memories will be tested according to U.S. Army Electronics Command specification SCS-517 (2/12/76) and will meet all electrical requirements of that specification.

SECTION III
MEETINGS

The post award meeting was held 6 October 1976 on site at Texas Instruments in Dallas, Texas by Mr. Dave Biser, Contract Monitor, and Mr. Bill Glendenning, technical advisor.